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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/818,263	03/26/2001	Hisanobu Ishiyama	81751.0011	9233

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EXAMINER

LAO, LUN YI

ART UNIT	PAPER NUMBER
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2673

DATE MAILED: 05/28/2003

12

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.
09/818,263

Applicant(s)
Ishiyama

Examiner
Lun-yi Lao

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on Apr 23, 2003.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-18 is/are pending in the application.
- 4a) Of the above, claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☒ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☒ All b) ☐ Some* c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- *See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). _____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____ 6) ☐ Other:

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DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the first paragraph of 35 U.S.C. 112:

The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

2. Claims 7-8 and 16 are rejected under 35 U.S.C. 112, first paragraph, as containing subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

The specification fails to disclose **how** the polarity inverting circuit having a shift register for inverting a polarity of a voltage applied to the liquid crystal layer in each row of scanning line since the applicants can shift register shift the same waveform to the opposite electrodes one by one(see figures 1-3 and page 18, lines 2-9). The specification only disclose the polarity inverting circuit(24) for inverting a polarity of a voltage applied to the opposite electrodes(C1-Cm) very frame(see figures 1-3 and page 19, lines 4-24).

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Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless -

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1, 2, 6, 9-11, 15 and 18 are rejected under 35 U.S.C. 102(b) as being anticipated by Iwasaki et al(5,774,099).

As to claims 1, 2, 6, 9-11, 15 and 18, Iwasaki et al teaches a liquid crystal device comprising a plurality of scanning lines(13); a plurality of data lines(14); a plurality of switching elements(26); a plurality of pixel electrodes connected to the plurality of switching elements(26); a plurality of row opposite electrodes(5, 6 or 29) arranged oppositely to the plurality of pixel electrodes through a liquid crystal layer; a scanning line driving circuit(9); a data line driving circuit(1-2, 2-1, 3-1, 3-2) and a polarity inverting circuit(64) for reversing a polarity of a voltage applied to the liquid crystal layer by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in synchronization with the scanning period(see figures 12, 5A, 5C; column 10, lines 13-23; column 11, lines 11-20; column 13, lines 47-68 and column 14, lines 1-51).

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As to claims 6 and 15, Iwasaki et al teach the polarity inverting circuit for reversing a polarity of a voltage applied to the liquid crystal layer ever one frame(odd frame and even frame)(see figures 5A and 5C).

5. Claims 1, 2, 6-11 and 15-18 are rejected under 35 U.S.C. 102(b) as being anticipated by Ishizaki et al(EP 0,558,059)

As to claims 1, 2, 6-11 and 15-18, Ishizaki et al teach a liquid crystal device comprising a plurality of scanning lines; a plurality of data lines; a plurality of switching elements(104); a plurality of pixel electrodes connected to the plurality of switching elements; a plurality of row opposite electrodes arranged oppositely to the plurality of pixel electrodes through a liquid crystal layer; a scanning line driving circuit(101); a data line driving circuit(102) and a polarity inverting circuit(103, 111) for reversing a polarity of a voltage applied to the liquid crystal layer by changing a voltage supplied to an opposite electrode of a row corresponding to the selected scanning line in synchronization with the scanning period(see figures 1-5; column 4, lines 16- 58; column 5, lines 1-58 and column 6, lines 1-2).

As to claims 6, 7 and 15-16, Ishizaki et al teach the polarity inverting circuit for reversing a polarity of a voltage applied to the liquid crystal layer ever one frame or every scanning line(see figures 2-5 and column 5, lines 45-58 and column 6, lines 1-2).

As to claims 8 and 17, Ishizaki et al teach M rows of opposite electrodes are insulated from each other(see figures 1 and 4).

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Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

7. Claims 3-5 and 12-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ishizaki et al (EP 0,558,059) in view of Hosokawa et al(4,393,380).

As to claims 3-5 and 12-14, Ishizaki et al teach a polarity inverting circuit(103, 111) comprising a shift register for shift a clock signal(see figures 1, 4 and column 4, lines 16-21). Ishizaki et al fail to disclose the polarity inverting circuit having a shift register for shift electric potential for applying to the row of opposite electrodes.

Hosokawa et al teach an LCD display having a common driver(34) having a shift register for performing a memory function(see figures 4, 7-9; column 7, lines 35-68 and column 8, lines 1-8). It would have been obvious to have modified Ishizaki et al with the teaching of Hosokawa et al, so as to simply the driving circuit.

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Response to Arguments

8. Applicant's arguments filed on April 23, 2003 have been fully considered but they are not persuasive.

Applicant argues that Iwasaki et al do not change a voltage applied to an opposite electrode of row corresponding to the selected scanning line in synchronization with the scanning period or every one frame on pages 4 and 5. The examiner disagrees with that since Iwasaki et al teaches the polarity of voltage(V_{comh} or V_{coml}) applied to the opposite row electrode(5 or 6) has been changed corresponding to the selected scanning line(13) in synchronization with the scanning period(frame period)(see figures 1, 5A, 5B; column 10, lines 13-23 and paragraph #4 above). Iwasaki et al teach the polarity of voltage(V_{comh}) has been applied to the opposite row electrode(5) in an odd frame and the opposite polarity of voltage(V_{coml})(see figures 5A, 5C and column 14, lines 1-3).

Applicant argues that Ishizaki et al do not change a voltage applied to an opposite electrode of row corresponding to the selected scanning line in synchronization with the scanning period on or every one frame pages 4 or 5. The examiner disagrees with that since Ishizaki et al the polarity of voltages(V_{c1} - V_{c3}) applied to the opposite row electrode have been changed corresponding to the selected scanning line in synchronization with the scanning period(frame period or line period)(see figures 1-5; column 5, lines 25-33 and lines 45-58; and column 6, lines 1-2).

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Applicant argues that Iwasaki et al do not invert a voltage applied to an opposite electrode for the respective rows in synchronization with a beginning of scanning period on pages 4-5).

The examiner disagrees with that since Iwasaki et al invert a voltage applied to an opposite electrode for the respective rows in synchronization with a beginning of scanning period(beginning of a frame period)(see figures 5A and 5C).

Applicant argues that Ishizaki et al do not invert a voltage applied to an opposite electrode for the respective rows in synchronization with a beginning of scanning period on pages 4-5).

The examiner disagrees with that since Ishizaki et al invert a voltage applied to an opposite electrode for the respective rows in synchronization with a beginning of scanning period(beginning of a frame period or a line period)(see figures 3-5; column 5, lines 25-33 and lines 45-58; and column 6, lines 1-2).

Applicant argues that Ishizaki et al does not teach the polarity inverting circuit inverts a polarity of voltage applied to the liquid crystal layer for each one of the M rows of scanning lines on page 5. The examiner disagrees with that since Ishizaki teach the polarity inverting circuit for reversing a polarity of a voltage applied to the liquid crystal layer every scanning line(see figures 2-5 and column 5, lines 45-58 and column 6, lines 1-2).

Applicant argues that Ishizaki et al does not teach the M rows of the opposite electrodes arranged oppositely a row of the MXN number of pixel electrodes in a rectangular shape, wherein the M rows of opposite electrodes are insulated from each other on page 6. The examiner disagrees with that since Ishizaki et al teach the M rows of the opposite electrodes arranged

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oppositely a row of the MXN number of pixel electrodes in a rectangular shape, wherein the M rows of opposite electrodes are insulated from each other(they are not crossing from each other, individual controlled by a switching circuit(110)(see figures 1 and 3) which is similar to applicant's opposite electrodes(C1-Cm) are not crossing from each other, but connected and controlled by a driving circuit(24)(see figures 1 and 2).

Applicant argues that the combination of Ishizaki and Hosokawa et al do not teach a memory section holds a first electric potential or second electric potential as an electric potential for each of the M rows of opposite electrodes and updates the held electric potential ever scanning period on pages 6-7. The examiner disagrees with that since Hosokawa et al teach a memory section(flip-flop) holds a first electric potential(first polarity of a potential) or second electric potential(second polarity of a potential) to as an electric potential for each of the rows of opposite electrodes and updates the held electric potential ever scanning period(frame period)(see figures 4, 7-9; column 7, lines 35-68 and column 8, lines 1-8).

Conclusion

9. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO

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MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lun-yi, Lao whose telephone number is (703) 305-4873.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala, can be reached at (703) 305-4938.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

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May 27, 2003

Lun-yi Lao
Lun-yi Lao

Primary Examiner